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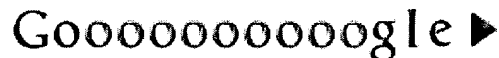
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This research addresses the need to consider details of the analog behavior of digital circuits and interconnect in order to ensure correct functionality. Specifically it focuses on analysis of timing and noise in deep submicron circuit designs. All noise sources in a digital integrated circuit are being considered - coupled and ringing noise on signal lines, power supply noise, and noise from the circuits. The effect of noise on delay is being considered in performance verification. Because many of the emerging timing and noise problems are associated with on-chip inductance, techniques for practically extracting on-chip inductance will be developed. The question of how the complex time-domain responses that result from inductive interconnect can be used in static timing and noise analysis is being investigated. Additional explorations are on using the complex time-domain responses that result from inductive interconnect for static timing and noise analysis. Other areas of investigation include a static solution to on-chip power grid integrity analysis and noise considerations in synthesis and circuit tuning. The educational plan includes building a VLSI CAD research laboratory, and development of courses in hardware design using FPGAs.

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Sankar Basu received Ph.D degree in electrical engineering from the University of Pittsburgh. Prior to joining NSF he was with the IBM T. J. Watson Research Center, NY for seven years. He has been a faculty member of EECS at the Stevens Institute of Technology, where he taught and conducted funded research (Air-Force, NSF), and for a brief period was with the Naval Underwater Systems center, CT as a visiting senior scientist. He has also visited the Ruhr University, Bochum, Germany as an Alexander von Humboldt fellow, and the MIT laboratory for Information and Decision Systems (LIDS) for extended periods. Dr. Basu's past research interests had been in the analytical aspects of multidimensional circuits, signals and systems. He has also worked on statistical learning, speech and multimedia signal processing and has, in addition, published on filter synthesis, image processing, nonlinear modeling techniques. An author/coauthor of over one hundred refereed publications including two special volumes on wavelets and filter banks, he was keynote speakers at the First Int. Workshops on n-D systems (NDS) 1998 in Lagow, Poland as well as at NDS2000 on Czocha Castle, Poland. He holds 5 US Patents with several more pending.

He has served as associate editors for the IEEE Transactions on Circuits and Systems, and the IEEE Transactions on Multimedia. He also serves on the editorial board of the Journal of Applied Signal Processing of the European Signal Processing Association, and the Journal of Multidimensional Systems and Signal Processing published by the Kluwer Academic Publishers. He has guest edited special issues of IEEE Transactions on Circuits and systems, IEEE Transactions on Multimedia, and Journal of VLSI Signal and Image Processing. Dr. Basu has organized, chaired sessions, and has been a panelist in many conferences in the areas of circuits and systems, statistical learning theory, and serves on multiple technical committees of IEEE societies in these fields. He was the general chair of first IEEE International Conference on Multimedia & Expo (ICME) 2000, for which he serves as the steering committee chair. He was an organizer for the NATO Advanced Study Institute on 'Statistical Learning and Applications' at the Katholieke University, Leuven, Belgium in July 2002.

He is an elected a Fellow of the IEEE for his 'contributions to the theory and application of multidimensional circuits systems and signal processing', and is a member of SIAM, Eta Kappa Nu

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